

## MGA-655T6

### Low Noise Amplifier with Bypass Mode in Low Profile Package

#### Description

Avago Technologies' MGA-655T6 is an economical easy-to-use GaAs MMIC Low Noise Amplifier (LNA) with Bypass mode. The Bypass mode enables the LNA to be bypassed during high input signal power and reduce current consumption. Its housed in a low profile 2 x 1.3 x 0.4mm 6-pin Ultra Thin Package.



Lifecycle status: **Active**



#### Features

- Broadband operation (2.5 – 4)GHz
- Adjustable bias current for gain/IP3 optimization
- Very low noise figure
- Bypass mode using a single pin
- Low current consumption in bypass mode, <100  $\mu$ A
- Fully matched to 50 ohm in bypass mode
- High Linearity in LNA and bypass mode
- GaAs E-pHEMT Technology[1]
- Low profile package size: 2.0 x 1.3 x 0.4 mm<sup>3</sup>
- Excellent uniformity in product specifications

#### Applications

- Low noise amplifier for Wimax, Wireless Local Loop

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### Data Sheet

#### Description

Avago Technologies' MGA-655T6 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA) with Bypass mode. The LNA has low noise and high linearity achieved through the use of Avago Technologies' proprietary 0.5  $\mu\text{m}$  GaAs Enhancement-mode pHEMT process. The Bypass mode enables the LNA to be bypassed during high input signal power and reduce current consumption. It is housed in a low profile 2 x 1.3 x 0.4 mm 6-pin Ultra Thin Package. The compact footprint and low profile coupled with low noise, high linearity make the MGA-655T6 an ideal choice as a low noise amplifier for mobile and CPE receivers in the WiMax and WLL (2.5-4) GHz band.

#### Component Image

2.0 x 1.3 x 0.4 mm<sup>3</sup> 6-Lead Ultra Thin Package



Note:

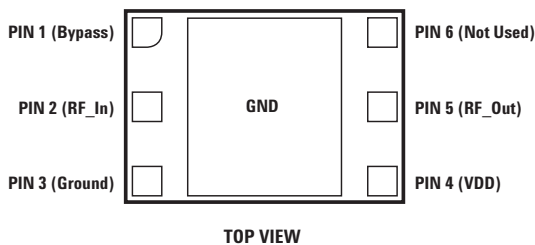
Package marking provides orientation and identification

"5F" = Product Code

"Y" = Year of Manufacture

"M" = Month of Manufacture

#### Pin Configuration



#### Features

- Low nominal operating current
- Simple input/output matching network
- Broadband operation (2.5 – 4 ) GHz
- Adjustable bias current for gain/IP3 optimization
- Very low noise figure
- Bypass mode using a single pin
- Low current consumption in bypass mode, <100  $\mu\text{A}$
- Fully matched to 50 ohm in bypass mode
- High Linearity in LNA and bypass mode
- GaAs E-pHEMT Technology<sup>[1]</sup>
- Low profile package size: 2.0 x 1.3 x 0.4 mm<sup>3</sup>
- Excellent uniformity in product specifications
- Tape-and-reel packaging option available

#### Typical Performance

- 3.5 GHz; Vdd = 3 V, Vbypass = 2.7 V (typ.), I<sub>ds</sub> = 10 mA (typ.)
- 14.7 dB gain
- 1.2 dB noise figure
- +5.5 dBm Input IP3
- -2 dBm input power at 1 dB gain compression
- 4.2 dB insertion loss in bypass mode
- 19 dBm IIP3 in bypass mode (pin = -20 dBm)
- <104  $\mu\text{A}$  current consumption in bypass & shutdown mode

#### Applications

- Low noise amplifier for Wimax, Wireless Local Loop
- Other ultra low noise applications in the (2.5 – 4) GHz band

Note:

1. Enhancement mode technology employs positive V<sub>gs</sub>, thereby eliminating the need of negative gate voltage associated with conventional depletion mode devices.



**Attention: Observe precautions for handling electrostatic sensitive devices.**

ESD Machine Model = 50 V

ESD Human Body Model = 200 V

Refer to Avago Technologies Application Note A004R:

*Electrostatic Discharge, Damage and Control.*

## Absolute Maximum Rating<sup>[1]</sup> $T_A = 25^\circ\text{C}$

| Symbol       | Parameter                              | Units            | Absolute Max. |
|--------------|--|------------------|---------------|
| $V_{dd}$     | Device Voltage, RF Output to Ground    | V                | 4             |
| $V_{bypass}$ | Control Voltage                        | V                | 4             |
| $P_{in,max}$ | CW RF Input Power                      | dBm              | +14           |
| $P_{diss}$   | Total Power Dissipation <sup>[3]</sup> | mW               | 66            |
| $T_j$        | Junction Temperature                   | $^\circ\text{C}$ | 150           |
| $T_{STG}$    | Storage Temperature                    | $^\circ\text{C}$ | -65 to 150    |

## Thermal Resistance<sup>[2,3]</sup>

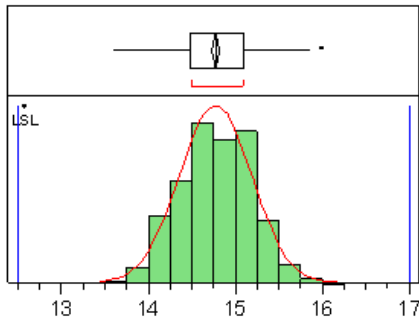
$(V_{dd} = 3.0\text{ V}, I_d = 10\text{ mA}), \theta_{jc} = 75^\circ\text{C/W}$

### Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red Measurement Technique.
3. For module substrate temperature,  $T_{sub}$ ,  $>94^\circ\text{C}$  derate the device power at 50 mW per  $^\circ\text{C}$  rise in board (module belly) temperature.

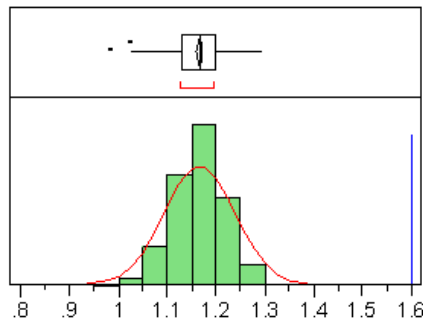
## Product Consistency Distribution Charts

**Process Capability for Gain**  
LSL=12.8, Nominal=14.7, USL=17



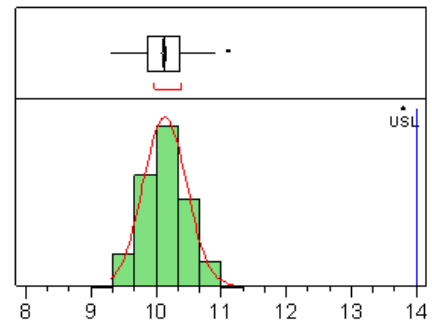
**Figure 1. Gain @ 3.5 GHz,  $V_d$  3 V;  $V_{bypass}$  2.7 V**

**Process Capability for NF**  
Nominal=1.2, USL=1.6



**Figure 2. NF @ 3.5 GHz,  $V_d$  3 V;  $V_{bypass}$  2.7 V**

**Process Capability for  $I_{ds}$**   
Nominal=10.1, USL=14



**Figure 3.  $I_{ds}$  @ 3.5 GHz,  $V_d$  3 V;  $V_{bypass}$  2.7 V**

### Note:

Distribution data sample size is 500 samples taken from 3 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.

## Electrical Specifications

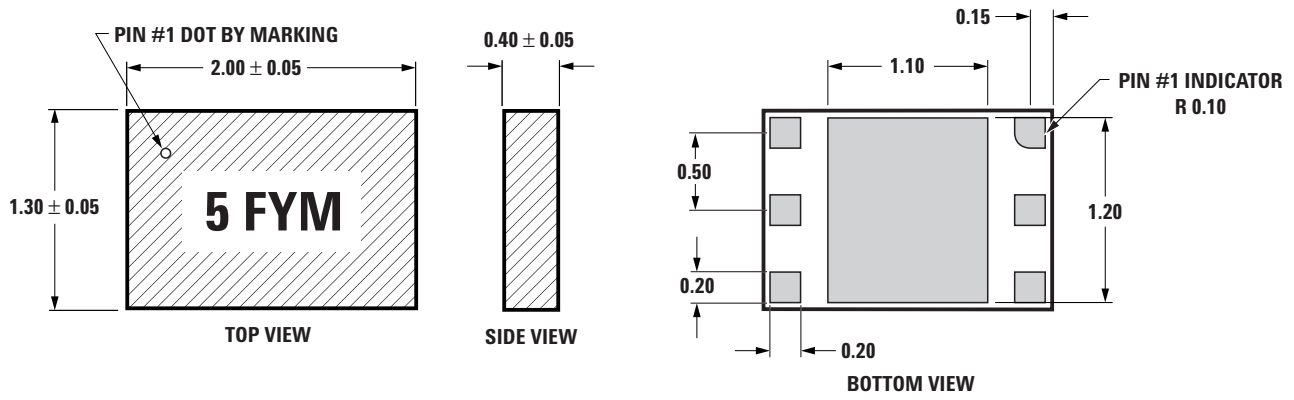
$T_A = 25^\circ\text{C}$ ,  $V_{dd} = 3\text{ V}$ ,  $V_{bypass} = 2.7\text{ V}$ ,  $I_{ds} = 10\text{ mA}$  (typ), RF measurement at 3.5 GHz, measured on demo board (see Fig. 4) unless otherwise specified.

| Symbol                       | Parameter and Test Condition                    | Units         | Min. | Typ.  | Max. |
|------------------------------|---|---------------|------|-------|------|
| Gain                         | Gain  | dB            | 12.8 | 14.7  | 17.0 |
| $I_d$                        | Bias Current                                    | mA            | -    | 10    | 14.0 |
| IIP3 [8]                     | Input Third Order Intercept Point               | dBm           | -    | +5.5  | -    |
| NF [9]                       | Noise Figure (Typ. $V_{bypass}=2.7\text{V}$ )   | dB            | -    | 1.2   | 1.6  |
| OP1dB                        | Output Power at 1dB Gain Compression            | dBm           | -    | +12   | -    |
| S11                          | Input Return Loss, 50 $\Omega$ source           | dB            | -    | -9    | -    |
| S22                          | Output Return Loss, 50 $\Omega$ load            | dB            | -    | -13.5 | -    |
| S12                          | Reverse Isolation                               | dB            | -    | -24.7 | -    |
| $ S_{21} ^2_{\text{BYPASS}}$ | Bypass Mode Loss ( $V_{bypass} = 0$ )           | dB            | -    | 4.2   | -    |
| IIP3 <sub>BYPASS</sub>       | Bypass Mode IIP3 (tested at -20dBm input Power) | dBm           | -    | + 19  | -    |
| $I_d_{\text{BYPASS}}$        | Bypass Mode current ( $V_{bypass} = 0$ )        | $\mu\text{A}$ | -    | 100   | -    |

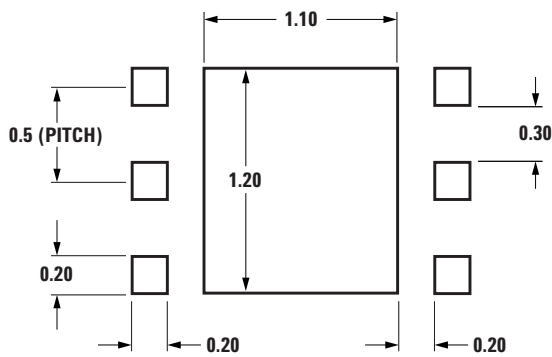
### Notes:

1. Measurements at 3.5 GHz obtained using demo board described in Figure 4, with component values on Figure 5.
2. 3.5 GHz IIP3 test condition:  $F_{RF1} = 3.50\text{ GHz}$ ,  $F_{RF2} = 3.505\text{ GHz}$  with input power of -20 dBm per tone.
3. Bypass Mode IIP3 test condition:  $F_{RF1} = 3.50\text{ GHz}$ ,  $F_{RF2} = 3.505\text{ GHz}$  with input power of -20 dBm per tone.

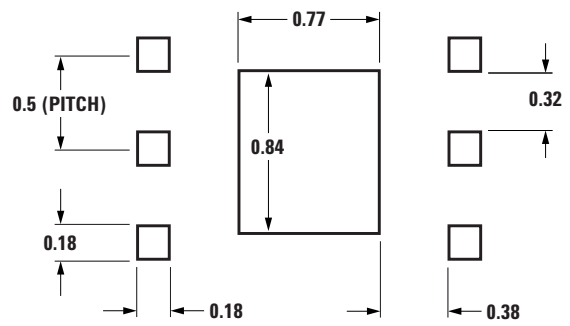
## Package Dimensions



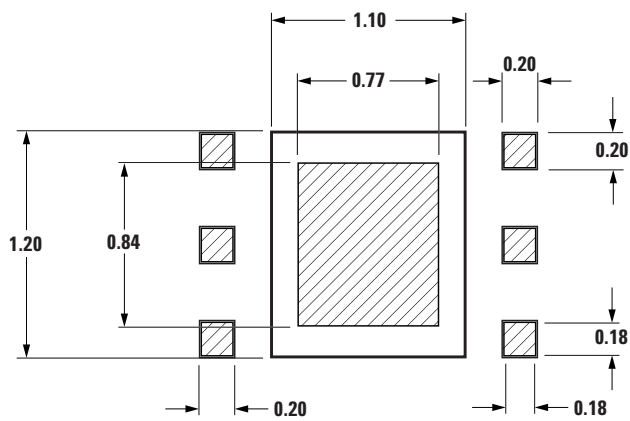
## PCB Land Patterns and Stencil Design



PCB Land Pattern (dimensions in mm)

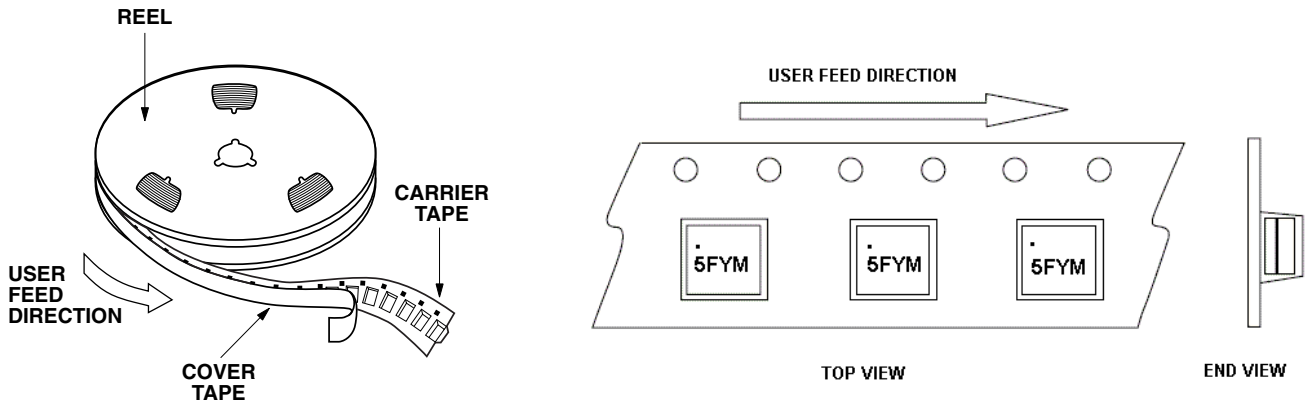


Stencil Outline Drawing (dimensions in mm)

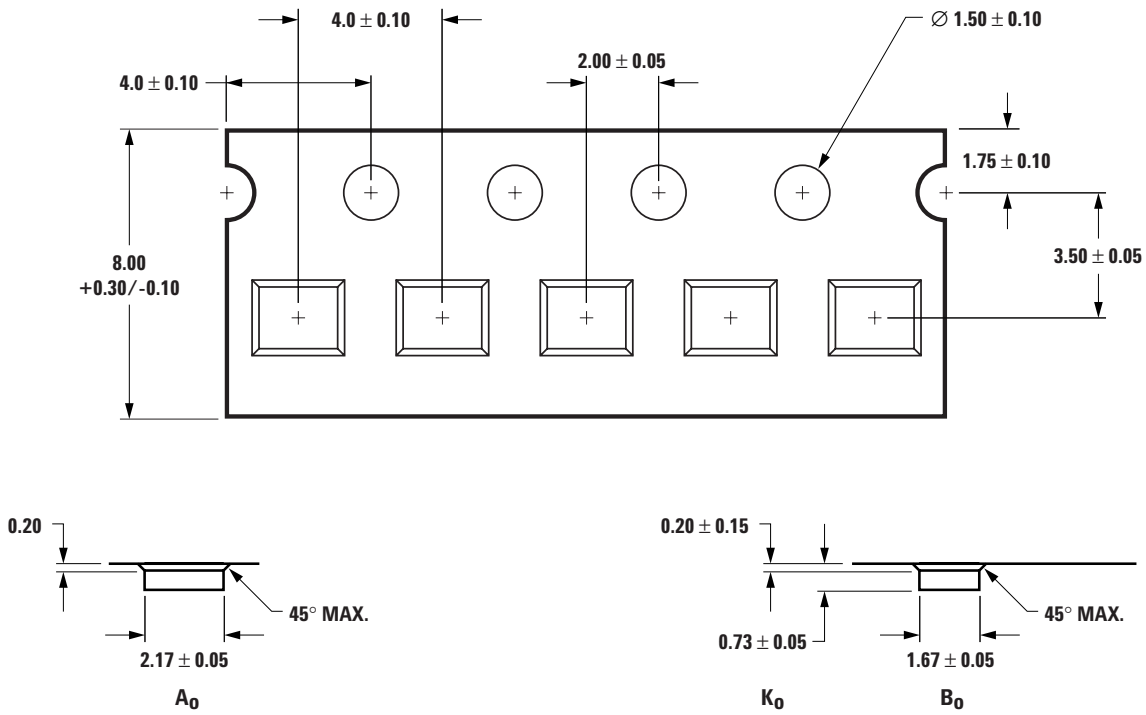


Combined PCB and Stencil Layouts (dimensions in mm)

## Device Orientation



## Tape Dimensions



## Part Number Ordering Information

| Part Number    | Quantity | Container      |
|----------------|----------|----------------|
| MGA-655T6-BLKG | 100      | Antistatic Bag |
| MGA-655T6-TR1G | 3000     | 7" Reel        |
| MGA-655T6-TR2G | 10000    | 13" Reel       |